Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims **1-24** (cancelled).

Please cancel claims **1-24** and add the following new claims **25 - 73**.

25 (new): A multi-chip electronic package comprising:

an organic, laminate chip carrier including a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material, said chip carrier including a plurality of electrical contacts on a first surface thereof and a plurality of electrical conductors on a second surface thereof, selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors;

a first, ASIC semiconductor chip positioned directly on said first surface of said organic, laminate chip carrier and electrically coupled to selected ones of said electrical contacts;

a second, memory semiconductor chip positioned on said first semiconductor chip such that said first and second semiconductor chips are in a stacked orientation, said second semiconductor chip electrically coupled to selected ones of said electrical contacts by a plurality of wirebond connections;

a stiffener member positioned on said first surface of said organic, laminate chip carrier and spacedly positioned about said first and second semiconductor chips; and

a heat-sinking member positioned on said stiffener member and substantially over said first and second semiconductor chips.

26 (new): The package of claim 25 wherein selected ones of said electrical contacts are electrically coupled to other selected ones of said electrical contacts such that said first and second semiconductor chips are electrically coupled to one another.

27 (new): The package of claim 25 wherein said first semiconductor chip is electrically coupled to selected ones of said electrical contacts by a plurality of solder balls.

28 (new): The package of claim 27 wherein said organic, laminate chip carrier includes a thermally conductive member therein, said thermally conductive member having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said electrical couplings formed by said solder balls on said selected ones of said electrical contacts.

29 (new): The package of claim 28 wherein said thermally conductive member is comprised of a first layer of copper, a second layer of an iron alloy and a third layer of copper.

30 (new): The package of claim 25 further including a quantity of encapsulant material located on said first surface of said organic, laminate chip carrier and substantially covering both said first and second semiconductor chips.

31 (new): The package of claim 25 further including an internal capacitor within said chip carrier.

32 (new): A multi-chip electronic package comprising:

an organic, laminate chip carrier including a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material, said chip carrier including a plurality of electrical contacts on a first surface thereof and a plurality of electrical conductors on a second surface thereof, selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors;

first and second semiconductor chips positioned on said first surface of said organic, laminate chip carrier in a stacked orientation, each semiconductor chip electrically coupled to selected ones of said electrical contacts, said chip carrier further including a first multilayered portion including at least one of said layers of dielectric material and at least one of said electrically conductive planes wherein said at least one of said electrically conductive planes of said first multilayered portion includes signal lines capable of having signals pass there-along at a first frequency and a second multilayered portion bonded to said first multilayered portion and adapted for having said first and second semiconductor chips coupled thereto, said second multilayered portion including at least one of said layers of dielectric material and at least one of said electrically conductive planes wherein said at least one of said electrically conductive planes of said second multilayered portion includes signal lines capable of having signals pass there-along at a higher frequency than said first frequency to thereby provide a high speed connection between said first and second semiconductor chips.

33 (new): The package of claim 32 wherein selected ones of said electrical contacts are electrically coupled to other selected ones of said electrical contacts such that said first and second semiconductor chips are electrically coupled to one another.

34 (new): The package of claim 32 wherein said first semiconductor chip is directly positioned on said first surface of said organic, laminate chip carrier and said second semiconductor chip is positioned on said first semiconductor chip.

35 (new): The package of claim 34 wherein said first semiconductor chip is an ASIC semiconductor chip and said second semiconductor chip is a memory chip.

36 (new): The package of claim 34 wherein said first semiconductor chip is electrically coupled to selected ones of said electrical contacts by a plurality of solder balls.

37 (new): The package of claim 36 wherein said organic, laminate chip carrier includes a thermally conductive member therein having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said electrical couplings formed by said solder balls on said selected ones of said electrical contacts.

38 (new): The package of claim 34 wherein said second semiconductor chip is electrically coupled to selected ones of said electrical contacts by a plurality of wirebond connections.

39 (new): The package of claim 32 further including a heat-sinking member positioned substantially over said first and second semiconductor chips.

40 (new): The package of claim 39 further including a stiffener member positioned on said first surface of said organic, laminate chip carrier and spacedly positioned about said first and second semiconductor chips, said heat sinking member being positioned on said stiffener member.

41 (new): The package of claim 32 further including a quantity of encapsulant material located on said first surface of said organic, laminate chip carrier and substantially covering both said first and second semiconductor chips.

42 (new): The package of claim 41 wherein said thermally conductive member is comprised of a first layer of copper, a second layer of an iron alloy and a third layer of copper.

43 (new): The package of claim 32 wherein said at least one electrically conducting plane of said second multilayered portion includes first and second layers of said dielectric material on opposite sides of said at least one conducting plane, and second and third electrically conductive planes each having signal lines on said first and second layers of said dielectric material, respectively.

44 (new): The package of claim 43 wherein said second multilayered portion further includes a conductive through hole interconnecting at least one of said signal lines of said second conductive plane with at least one of said signal lines of said third conductive plane.

45 (new): The package of claim 32 wherein said organic, laminate chip carrier includes an internal capacitor therein.

46 (new): A method of making a multi-chip electronic package, said method comprising:

providing an organic, laminate chip carrier including a first surface and a second surface and a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material;

providing a plurality of electrical contacts on said first surface of said chip carrier and a plurality of electrical conductors on said second surface of said chip carrier, selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors;

positioning a first, ASIC semiconductor chip directly on said first surface of said chip carrier and electrically coupling said first, ASIC semiconductor chip to selected ones of said electrical contacts;

positioning a second, memory semiconductor chip on said first, ASIC semiconductor chip such that said first and second semiconductor chips are in a stacked orientation;

electrically coupling said second semiconductor chip to selected ones of said electrical contacts by a plurality of wirebond connections;

positioning a stiffener member on said first surface of said chip carrier in a spaced orientation about said first and second semiconductor chips; and

positioning a heat-sinking member on said stiffener member and substantially over said first and second semiconductor chips.

47 (new): The method of claim 46 further including electrically coupling selected ones of said electrical contacts to other selected ones of said electrical contacts such that said first and second semiconductor chips are electrically coupled to one another.

48 (new): The method of claim 46 wherein said electrical coupling of said first semiconductor chip to selected ones of said electrical contacts is accomplished using a plurality of solder balls.

49 (new): The method of claim 48 further including providing a thermally conductive member within said chip carrier having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said electrical couplings formed by said solder balls on said selected ones of said electrical contacts.

50 (new): The method of claim 46 further including positioning a quantity of encapsulant material on said first surface of said organic, laminate chip carrier to substantially cover both said first and second semiconductor chips.

51 (new): The method of claim 46 further including providing an internal capacitor within said chip carrier.

52 (new): A method of making a multi-chip electronic package, said method comprising:

providing an organic, laminate chip carrier including first and second surfaces and a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material:

providing a plurality of electrical contacts on said first surface of said chip carrier and a plurality of electrical conductors on said second surface of said chip carrier; selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors;

positioning first and second semiconductor chips on said first surface of said chip carrier in a stacked orientation and electrically coupling said first and second semiconductor chips to selected ones of said electrical contacts, said chip carrier further including a first multilayered portion including at least one of said layers of dielectric material and at least one of said electrically conductive planes

wherein said at least one of said electrically conductive planes of said first multilayered portion includes signal lines capable of having signals pass there-along at a first frequency and a second multilayered portion bonded to said first multilayered portion and adapted for having said first and second semiconductor chips coupled thereto, said second multilayered portion including at least one of said layers of dielectric material and at least one of said electrically conductive planes wherein said at least one of said electrically conductive planes of said second multilayered portion includes signal lines capable of having signals pass there-along at a higher frequency than said first frequency to thereby provide a high speed connection between said first and second semiconductor chips.

53 (new): The method of claim 52 further including electrically coupling selected ones of said electrical contacts to other selected ones of said electrical contacts such that said first and second semiconductor chips are electrically coupled to one another.

54 (new): The method of claim 52 wherein said first semiconductor chip is directly positioned on said first surface of said organic, laminate chip carrier and said second semiconductor chip is positioned on said first semiconductor chip.

55 (new): The method of claim 52 wherein said electrical coupling of said first semiconductor chip to selected ones of said electrical contacts is accomplished using a plurality of solder balls.

56 (new): The method of claim 55 further including providing a thermally conductive member within said chip carrier having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said electrical couplings formed by said solder balls on said selected ones of said electrical contacts.

57 (new): The method of claim 52 wherein said electrical coupling of said second semiconductor chip to said selected ones of said electrical contacts is accomplished using a plurality of wirebond connections.

58 (new): The method of claim 52 further including positioning a stiffener member on said first surface of said carrier in a spaced orientation about said first and second semiconductor chips.

59 (new): The method of claim 58 further including positioning a heat-sinking member on said stiffener member substantially over said first and second semiconductor chips.

60 (new): The method of claim 52 further including positioning a quantity of encapsulant material on said first surface of said chip carrier substantially covering both said first and second semiconductor chips.

61 (new): The method of claim 52 further including providing first and second layers of said dielectric material on opposite sides of said at least one conducting plane within said second multilayered portion, and providing second and third electrically conductive planes each having signal lines on said first and second layers of said dielectric material, respectively.

62 (new): The method of claim 61 further including providing a conductive through hole within said second multilayered portion interconnecting at least one of said signal lines of said second conductive plane with at least one of said signal lines of said third conductive plane.

63 (new): The method of claim 52 further including providing an internal capacitor within said chip carrier.

64 (new): A multi-chip electronic package assembly comprising:

a circuitized substrate including a plurality of electrically conductive members thereon;

an organic, laminate chip carrier including a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material, said chip carrier including a plurality of electrical contacts on a first surface thereof and a plurality of electrical conductors on a second surface thereof, selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors;

a first, ASIC semiconductor chip positioned directly on said first surface of said organic, laminate chip carrier and electrically coupled to selected ones of said electrical contacts;

a second, memory semiconductor chip positioned on said first semiconductor chip such that said first and second semiconductor chips are in a stacked orientation, said second semiconductor chip electrically coupled to selected ones of said electrical contacts by a plurality of wirebond connections;

a stiffener member positioned on said first surface of said organic, laminate chip carrier and spacedly positioned about said first and second semiconductor chips;

a heat-sinking member positioned on said stiffener member and substantially over said first and second semiconductor chips; and

a plurality of electrically conductive elements electrically connecting said selected ones of said electrical conductors on said second surface of said organic, laminate chip carrier to respective ones of said electrically conductive members on said circuitized substrate.

65 (new): The assembly of claim 64 wherein said circuitized substrate comprises a printed circuit board.

66 (new): The assembly of claim 64 wherein said plurality of electrically conductive elements comprises a plurality of solder members.

67 (new): The assembly of claim 64 further including a first plurality of solder balls electrically coupling said first semiconductor chip to selected ones of said plurality of electrical contacts on said first surface of said laminate chip carrier.

68 (new): The assembly of claim 64 further including a plurality of wirebond connections electrically coupling said second semiconductor chip to other selected ones of said plurality of electrical contacts on said first surface of said laminate chip carrier.

69 (new): A multi-chip electronic package assembly comprising:

a circuitized substrate including a plurality of electrically conductive members thereon;

an organic, laminate chip carrier including a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material, said chip carrier including a plurality of electrical contacts on a first surface thereof and a plurality of electrical conductors on a second surface thereof, selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors;

first and second semiconductor chips positioned on said first surface of said organic, laminate chip carrier in a stacked orientation, each semiconductor chip electrically coupled to selected ones of said electrical contacts, said chip carrier

further including a first multilayered portion including at least one of said layers of dielectric material and at least one of said electrically conductive planes wherein said at least one of said electrically conductive planes of said first multilayered portion includes signal lines capable of having signals pass there-along at a first frequency and a second multilayered portion bonded to said first multilayered portion and adapted for having said first and second semiconductor chips coupled thereto, said second multilayered portion including at least one of said layers of dielectric material and at least one of said electrically conductive planes wherein said at least one of said electrically conductive planes of said second multilayered portion includes signal lines capable of having signals pass there-along at a higher frequency than said first frequency to thereby provide a high speed connection between said first and second semiconductor chips; and

a plurality of electrically conductive elements electrically connecting said selected ones of said electrical conductors on said second surface of said organic, laminate chip carrier to respective ones of said electrically conductive members on said circuitized substrate.

70 (new): The assembly of claim 69 wherein said circuitized substrate comprises a printed circuit board.

71 (new): The assembly of claim 69 wherein said plurality of electrically conductive elements comprises a plurality of solder members.

72 (new): The assembly of claim 69 further including a first plurality of solder balls electrically coupling said first semiconductor chip to selected ones of said plurality of electrical contacts on said first surface of said laminate chip carrier.

73 (new): The assembly of claim 69 further including a plurality of wirebond connections electrically coupling said second semiconductor chip to other selected ones of said plurality of electrical contacts on said first surface of said laminate chip carrier.